120

AF 2800

Docket No.: GR 98 P 2651

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

MAIL STOP: APPEAL BRIEF-PATENTS

By: Nathan Wolff Date: January 16, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

Applic. No.	:	09/816,927 Confirmation No.: 6167
Inventor	:	Heinrich Brunner et al.
Filed	:	March 23, 2001
Title	:	Semiconductor Component Having Field-Shaping Regions
TC/A.U.	:	2822
Examiner	:	Kiesha L. Rose
Docket No.	:	GR 98 P 2651
Customer No.	:	24131

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated July 18, 2003, finally rejecting claims 1-20.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $330.00 to cover the fee for filing the *Brief on Appeal*.

01/23/2004 TLUU11 00000028 09816927
01 FC:1402 330.00 OP

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-20 are rejected and are under appeal. No claims were cancelled or withdrawn from consideration.

Status of Amendments:

No claims were amended after the final Office action. *A Response under 37 CFR § 1.116* was filed on October 15, 2003. The Examiner stated in an *Advisory Action* dated November 18, 2003, that the request for reconsideration had been considered but did not place the application in condition for allowance.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to a semiconductor component having a semiconductor

body of a first conductivity type, that has a doping concentration of more than 5 x 10^{13} charge carriers per cm^3 and is provided with in each case at least one electrode on two mutually opposite surfaces. At least one of the electrodes makes contact with a semiconductor zone of a second conductivity type opposite to the first conductivity type. The invention relates in particular to an edge structure for such a semiconductor component.

Appellants stated on page 15 of the specification, line 16, that, in the figures, corresponding parts are respectively provided with the same reference symbols. Moreover, in the figures not all of the sectional parts are hatched, for the sake of better illustration. It is also noted that the respective conductivity types illustrated in the exemplary embodiments can, of course, be reversed.

If is further explained on page 15 of the specification, line 23, that, referring now to the figures of the drawings in detail and first, particularly, to Fig. 1 thereof, there is shown a semiconductor body 1 including an n^+-conducting semiconductor substrate 2 and an n^--conducting semiconductor layer 3 having a basic doping which is 5 x 10^{13} charge carriers cm^{-3} or more.

Appellants outlined on page 16 of the specification, line 4, that a cathode K is connected to the semiconductor substrate 2, while an anode A is connected to a p^+-conducting zone 4.

Appellants also stated on page 16 of the specification, line 7, that field plates 5 are provided on the top side of the semiconductor body 1 on or in an insulating layer (not specifically illustrated) made of silicon dioxide, for example. Moreover, an n^+-conducting guard ring 6 is additionally embedded in that surface of the semiconductor body 1 which faces the field plates 5. This guard ring 6, like the field plates 5, serves for increasing the breakdown strength of the diode in the edge region thereof.

It is further outlined on page 16 of the specification, line 16, that the invention then provides p-conducting regions 7, which surround the zone 4 at a distance in a well-shaped manner and are interrupted by channels 8 in the drift region below the zone 4, through which channels the operating current can flow between anode A and cathode K.

It is explained in the last paragraph on page 16 of the specification, line 22, that the regions 7 are so highly doped that they are not completely depleted of charge carriers in

the case of reverse-biasing when the reverse voltage is applied between anode A and cathode K.

Appellants outlined on page 17 of the specification, line 1, that Fig. 2 shows a further exemplary embodiment of the invention, which differs from the exemplary embodiment of Fig. 1 by the fact that here the regions 7 are interrupted in the edge region, too, by a multiplicity of channels 8. A "field strength trapezoid" is also indicated here diagrammatically on one of the channels 8, by a broken line 9. The length of this field strength trapezoid is determined by the length of the semiconductor body 1 between the regions 7, that is to say by the width of the channel 8 of the first conductivity type. In other words, the length of the field strength trapezoid depends on the distance between two adjacent regions of the second conductivity type. By correspondingly increasing the number of regions 7 of the second conductivity type, it is thus possible to string together practically any desired number of field strength trapezoids, which leads to a corresponding increase of the reverse voltage.

Appellants stated in the last paragraph on page 17 of the specification, line 18, that Fig. 3 shows a further exemplary embodiment of the invention, in which - in a similar manner to the exemplary embodiment of Fig. 1 - the p-conducting regions

7 are continuous in the edge region, with the result that there are channels 8 only in the drift region of the diode. Moreover, an insulating zone 10 made of silicon dioxide, for example, is additionally provided here, which insulating zone annularly surrounds the region below the zone 4 and shields charge carriers from the edge region. Accordingly, field plates 5 are not provided in this exemplary embodiment.

Appellants explained on page 18 of the specification, line 4, that Fig. 4 shows a MOS field-effect transistor having an emitter electrode E, a gate electrode G and a collector electrode C. The collector electrode C is connected to a p^+-conducting zone 11, while the emitter electrode E is connected to a p-conducting zone 12 and an n-conducting zone 13 and the gate electrode G lies above the channel region formed by the zone 12 and is isolated in a customary manner from the semiconductor body by an insulating layer, for example, made of silicon dioxide. In this exemplary embodiment, in a similar manner to Fig. 2, the p-conducting regions 7 surround the zones 12 and 13 at a respective distance in a well-shaped manner and are in this case each isolated by channels 8 of the semiconductor body 2. Moreover field plates 5 for increasing the breakdown strength are additionally provided in the edge region of this MOS field-effect transistor.

Appellants further stated on page 18 of the specification, line 20 that Fig. 5 shows a further exemplary embodiment of the invention with a MOS field-effect transistor which corresponds to the MOS field-effect transistor of Fig. 4 but has no field plates 5.

Appellants outlined on page 19 of the specification, line 1, that, as is shown in Fig. 1 and 2, the field plates 5 can be connected to the p-conducting regions 5. However, they can also be floating, as is illustrated in Fig. 4.

As further outlined on page 19 of the specification, line 5, Fig. 6 shows a further exemplary embodiment of the invention, in which the semiconductor body includes, instead of the semiconductor layer 3, a plurality of differently doped epitaxial layers 16, 17 and 18, between each of which the regions 7 are introduced for example by ion implantation. In this connection, it should be noted that in the previous exemplary embodiments of Figs. 1 to 5, too, the individual regions 5 can be produced by corresponding deposition of individual, identically doped layers and ion implantation steps. Moreover, a source metallization layer 19 connected to a terminal S, an insulating layer 20 made of silicon dioxide, gate electrodes 21 made, for example, of doped polycrystalline silicon and a p-conducting zone 22 are additionally shown in

the exemplary embodiment of Fig. 6. Instead of this p-conducting zone 22, it is also possible to provide a weak injector, for example a Schottky barrier layer. This zone 22 can have the same layer thickness as the substrate 2 or be thicker than the latter. Adjacent to the substrate layer 2 is a layer 14, which is connected to a terminal D.

References Cited:

U.S. Patent No. 5,113,237 (*Stengl*), dated May 12, 1992;

U.S. Patent No. 5,175,598 (*Nishizawa et al.*), dated December 29, 1992;

U.S. Patent No. 5,324,971 (*Notley*), dated June 28, 1994;

U.S. Patent No. 5,945,701 (*Siergiej et al.*), dated August 31, 1999.

Issues

1. Whether or not claims 1-3, 5-7, 10-14, 16-17, and 20 are obvious over *Nishizawa et al.* in view of *Stengl* under 35 U.S.C. §103.

2. Whether or not claims 4 and 15 are obvious over *Nishizawa et al.* and *Stengl* in view of *Siergiej et al.* under 35 U.S.C. §103.

3. Whether or not claims 8-9 and 18-19 are obvious over *Nishizawa et al.* and *Stengl* in view of *Notley* under 35 U.S.C. §103.

Grouping of Claims:

Claims 1 and 11-12 are independent. Claims 2-10 depend on claim 1 and claims 13-20 depend on claim 12. The patentability of dependent claims 2-10 and 13-20 is not separately argued. Therefore, claims 2-10 and 13-20 stand or fall with claims 1 and 12, respectively.

Arguments:

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 12 (similarly claims 1 and 11) calls for, inter alia:

> each one of said semiconductor regions ***being interrupted*** at at least one location ***by channels*** formed by said semiconductor body, said ***channels electrically connecting parts of said semiconductor body*** separated by said semiconductor regions

In the *Advisory Action* dated November 18, 2003, the Examiner stated that:

> ... the arguments filed are not found to be persuasive as stated in the previous office action filed 18 July 2003, which stated that the Nishizawa reference does disclose channel regions that surround the semiconductor body and semiconductor regions. Therefore the rejection stands.

The Examiner stated in the third paragraph on page 3 of the Office action dated July 18, 2003, that:

> Nishizawa discloses all of the limitations except for the semiconductor body having a doping concentration greater than 5 x 10^{13} charge carrier cm^{-3}. Whereas Stengl discloses ... a semiconductor body (1) with a doping concentration of 10^{18} cm^{-3} to properly form conductive regions.

In col. 2, lines 54-59, *Nishizawa et al.* state:

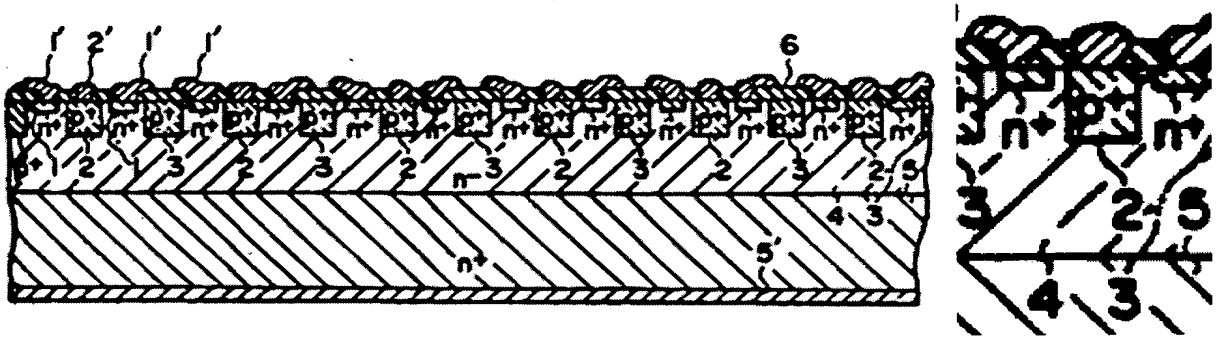
> In the vicinity of the upper surface of the n.sup.- type semiconductor layer 4, there is disposed a heavily doped p.sup.+ type semiconductor region 3 which has a grid-like shape as shown in FIG. 1 so as to surround a plurality of individual portions of the n.sup.- type semiconductor layer 4.

(Emphasis added.)

Nishizawa et al. do not disclose or suggest a semiconductor region of a second conductivity type (semiconductor region 3 of *Nishizawa et al.*) ***surrounding*** a semiconductor zone formed of a semiconductor of a first conductivity type (individual portions of the semiconductor layer 4 of *Nishizawa et al.*) ***except*** for a channel formed of the semiconductor of a first conductivity type, otherwise being electrically separated from each other by the semiconductor regions.

The lack of "channels" (formed of the semiconductor layer 4 of *Nishizawa et al.)* can be clearly seen in Fig. 2 of *Nishizawa et al.*, reproduced below together with an enlarged section thereof.

FIG. 2



The inventive concept of the invention of the instant application is to avoid large reverse currents despite high applied voltages by using a semiconductor component having a semiconductor layer with a doping concentration greater than 5 x 10^{13} charge carriers cm^{-3} in combination with a semiconductor region of a second conductivity type ***surrounding*** the semiconductor zone formed of a semiconductor of a first conductivity type ***except*** for a channel formed of the semiconductor of a first conductivity type. The applied references neither suggest nor contain the relevant teaching that would suggest such a semiconductor component. Therefore, the invention as recited in claims 1, 11, and 12 of the instant application is also believed not to be obvious over the cited references.

It is accordingly believed to be clear that *Nishizawa et al.* in view of *Stengl* do not suggest the features of claims 1, 11, and 12. Claims 1, 11, and 12 are, therefore, believed to be patentable over the art and since claims 2-10 and 13-20 are ultimately dependent on either of claims 1 and 12, they are believed to be patentable as well.

In the last paragraph on page 3 of the Office action, claims 4 and 15 have been rejected as being obvious over *Nishizawa et al.* and *Stengl* in view of *Siergiej et al.* (US 5,945,701) under 35 U.S.C. § 103.

In the second paragraph on page 4 of the Office action, claims 8-9 and 18-19 have been rejected as being obvious over *Nishizawa et al.* and *Stengl* in view of *Notley* (US 5,324,971) under 35 U.S.C. § 103.

Considering the deficiencies of the primary reference *Nishizawa et al.*, it is believed not to be necessary at this stage to address in more detail the secondary reference *Stengl* or the secondary references *Siergiej et al. and Notley* applied in the above-noted rejection of certain dependent claims, and whether or not there is sufficient suggestion or motivation

with a reasonable expectation of success for modifying or combining the references as required by MPEP § 2143.

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

Markus Nolff (Reg. No. 37,006)

MN/bb

Date: January 16, 2004
Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, Florida 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Appendix - Appealed Claims:

1. A semiconductor component, comprising:

a semiconductor body of a first conductivity type, said semiconductor body having a first doping concentration greater than 5 x 10^{13} charge carriers cm^{-3} and having a first surface and a second surface, said first and second surfaces being provided opposite from one another;

at least a first electrode disposed on said first surface and at least a second electrode disposed on said second surface;

a semiconductor zone of a second conductivity type opposite to the first conductivity type;

a pn-junction formed between said semiconductor zone of the second conductivity type and said semiconductor body;

at least one of said first and second electrodes being in contact with said semiconductor zone of the second conductivity type;

semiconductor regions of the second conductivity type provided in said semiconductor body;

said semiconductor regions being disposed at a respective distance from said semiconductor zone of the second conductivity type such that said semiconductor regions

surround said semiconductor zone of the second conductivity type in a well-shape;

each one of said semiconductor regions being interrupted at at least one location by channels formed by said semiconductor body, said channels electrically connecting parts of said semiconductor body separated by said semiconductor regions; and

said semiconductor regions of the second conductivity type having a second doping concentration such that said semiconductor regions are not completely depleted of charge carriers in case of a reverse-biasing of said pn-junction.

2. The semiconductor component according to claim 1, wherein each one of said semiconductor regions of the second conductivity type are interrupted at a plurality of locations by said channels formed by said semiconductor body for increasing a reverse voltage.

3. The semiconductor component according to claim 1, wherein said channels are configured such that electric field spikes are avoided when a reverse voltage is applied between said first and second electrodes.

4. The semiconductor component according to claim 1, wherein:

said semiconductor body has a drift region; and

said channels are provided in said drift region.

5. The semiconductor component according to claim 1, wherein:

said semiconductor body has an edge region; and

said channels are provided in said edge region.

6. The semiconductor component according to claim 1, wherein:

said semiconductor body has an edge zone; and

an insulating zone is provided for shielding charge carriers from said edge zone.

7. The semiconductor component according to claim 1, including an injector disposed in at least one of said first and second surfaces.

8. The semiconductor component according to claim 1, wherein:

one of said first and second surfaces surrounds said semiconductor zone of the second conductivity type; and

field plates are provided on said one of said first and second surfaces.

9. The semiconductor component according to claim 1, wherein:

said semiconductor body has an edge; and

a doped guard ring zone of the first conductivity type surrounds said edge.

10. The semiconductor component according to claim 1, wherein the first conductivity type is an n-conductivity type.

11. A semiconductor configuration, comprising:

a semiconductor component selected from the group consisting of a diode, a MOS transistor and a thyristor;

said semiconductor component including:

a semiconductor body of a first conductivity type, said semiconductor body having a first doping concentration greater than 5×10^{13} charge carriers cm^{-3} and having a first

surface and a second surface, said first and second surfaces being provided opposite from one another;

at least a first electrode disposed on said first surface and at least a second electrode disposed on said second surface;

a semiconductor zone of a second conductivity type opposite to the first conductivity type;

a pn-junction formed between said semiconductor zone of the second conductivity type and said semiconductor body;

at least one of said first and second electrodes being in contact with said semiconductor zone of the second conductivity type;

semiconductor regions of the second conductivity type provided in said semiconductor body;

said semiconductor regions being disposed at a respective distance from said semiconductor zone of the second conductivity type such that said semiconductor regions surround said semiconductor zone of the second conductivity type in a well-shape;

each one of said semiconductor regions being interrupted at at least one location by channels formed by said semiconductor body, said channels electrically connecting

parts of said semiconductor body separated by said semiconductor regions; and

said semiconductor regions of the second conductivity type having a second doping concentration such that said semiconductor regions are not completely depleted of charge carriers in case of a reverse-biasing of said pn-junction.

12. A semiconductor component, comprising:

a semiconductor body having a semiconductor layer of a first conductivity type with a doping concentration greater than 5 x 10^{13} charge carriers cm^{-3};

a semiconductor zone of a second conductivity type opposite to said semiconductor layer of said first conductivity type;

a pn-junction formed between said semiconductor zone and said semiconductor layer; and

semiconductor regions of the second conductivity type in said semiconductor body, said semiconductor regions surrounding said semiconductor zone at a respective distance except for a channel formed of said semiconductor layer interrupting each respective one of said semiconductor regions and electrically connecting parts of said semiconductor body separated by said semiconductor regions, said semiconductor regions having a

doping concentration preventing completely depleted of charge carriers upon a reverse-biasing of said pn-junction.

13. The semiconductor component according to claim 12, wherein said channel is one of a plurality of channels for increasing a reverse voltage.

14. The semiconductor component according to claim 12, wherein said channel is configured such that electric field spikes are avoided when a reverse voltage is applied between said semiconductor zone and said semiconductor body.

15. The semiconductor component according to claim 12, wherein said semiconductor body has a drift region and said channel is provided in said drift region.

16. The semiconductor component according to claim 12, wherein said semiconductor body has an edge region and said channel is provided in said edge region.

17. The semiconductor component according to claim 12, wherein said semiconductor body has an edge zone and an insulating zone is provided for shielding charge carriers from said edge zone.

18. The semiconductor component according to claim 12, wherein said semiconductor body has a first surface and a second surface, one of said first and second surfaces surrounds said semiconductor zone of the second conductivity type, and field plates are provided on said one of said first and second surfaces.

19. The semiconductor component according to claim 12, wherein said semiconductor body has an edge, and a doped guard ring zone of the first conductivity type surrounds said edge.

20. The semiconductor component according to claim 12, wherein the first conductivity type is an n-conductivity type.